REMARKS

Claims 1-21 are pending in this application. Claims 1 and 12 are amended herein. Applicant respectfully requests reconsideration of the claims in view of the following remarks.

Claim 11 was rejected under 35 U.S.C. § 112 second paragraph as being indefinite for failing to particularly point out and distinctly claim the subject matter regarded as the invention. This rejection is hereby respectfully traversed.

The Examiner remarks that the language "post-fabrication stress test" is not clear or distinct, and further the Examiner remarks that the term is not defined, asking whether it is a well known term.

Applicant replies that the term includes a first descriptive limitation that is very clear. "Post-fabrication" clearly means after fabrication. Thus a "post-fabrication stress test" is clearly a "stress test performed" after fabrication. The term is used in the specification and the claim identically and is therefore supported.

Further the term "stress test" is a term of art. Stress tests of fabricated integrated circuits are well known and stress test is a term well known in that art. The McGraw-Hill Dictionary of Scientific and Technical Terms, Fourth Edition, Copyright 1989, McGraw Hill, provides the following definition at page 1837:

> Stress test [ENG] A test of equipment under extreme conditions, outside the range anticipated in normal operation.

U.S. Patent No. 6,577,546 B2, also cited in the attached Information Disclosure Statement, also discloses stress tests run on an integrated circuit DRAM, a mode of operation for the I.C. is a "stress test" mode (Col. 4, lines 57-67).

Applicant submits that one skilled in the art knows precisely what is meant by the method steps of claim 11, and that the claim is definite as required by §112 second paragraph. Reconsideration and allowance are therefore requested.

Claims 1-4, 6, 8-15, 17, and 20-21 were rejected under 35 U.S.C. § 102(e) as being anticipated by Burgan, U.S. Patent No. 6,778,457. This rejection is hereby respectfully traversed.

Claim 1 is amended herein and now recites in part:

> ...storing information for distinguishing between a first portion of a DRAM comprising a plurality of volatile memory cells requiring refresh at a first rate and a second portion of said DRAM comprising a differing plurality of volatile memory cells permitting refresh at a second rate lower than said first rate; and
>
> accessing said stored information to refresh said first portion at said first rate and to refresh said second portion at said second rate.

Applicant respectfully submits that the reference, Burgan, does not show, teach or suggest the above recited methods of claim 1. In particular, the reference does not show, teach or suggest the steps of "storing information for distinguishing between a first portion of DRAM comprising a plurality of volatile memory cells requiring refresh at a first rate and a second portion of said DRAM comprising a differing plurality of volatile memory cells permitting refresh at a second rate lower than the first..." and "accessing said stored information to refresh said first portion at said first rate and to refresh said second portion at said second rate."

Burgan teaches providing a memory array and separately providing a plurality of test cells each having a memory cell. The test cells may be refreshed at differing rates and a monitor circuit adjusts the refresh rate of the memory array based on the stored logic status of the test cells. (Abstract). The Examiner asserted that Burgan's test cells provide a first portion and a second portion and that the monitor circuit refreshes the portions at a first rate and a second rate.

Applicant has examined the reference in light of the Examiner's remarks; and finds that the Burgan reference does not solve the same problem nor does it disclose the methods advantageously provided by Applicant's claimed method. Burgan discloses providing test cells including a single capacitor storage element in the refresh control circuitry. The test cells are refreshed at differing rates and the logic state of the cells is monitored by a monitor circuit. Based on the leakage of stored charge from the test cells, a DRAM array is refreshed at a rate sufficient to avoid loss of stored charge in the memory cells of that array.

Applicant finds no disclosure of "storing information to distinguish between a first portion of a DRAM ...and a second portion of a DRAM" each comprising a plurality of volatile memory cells. In contrast to the advantageous method of Applicant's claims, the reference teaches a DRAM array that requires refresh and test cells for determining and adapting a single refresh rate to be applied to the DRAM array. The test cells identified by the Examiner as the first and second portions are in fact part of the refresh controller circuitry, not the DRAM array being refreshed. Burgan adapts a single refresh rate for his DRAM array and does not provide differing refresh rates for portions of a DRAM array, each comprising a plurality of memory cells.

Applicant concludes that the method steps of claim 1 are not anticipated, or obviated, by the reference and are therefore allowable. Reconsideration and allowance for the method of claim 1 is therefore respectfully requested.

Claim 12 is an analogous apparatus claim to an integrated circuit comprising the first and second portions of a DRAM, which also stores information to distinguish the portions and refreshes the portions at a first and second refresh rate. Like claim 1, claim 12 is amended herein. Applicant believes that the Burgan reference does not show, teach or suggest the

elements of claim 12 and that claim 12 is therefore allowable. Reconsideration and allowance are requested for claim 12.

Claims 2 and 13 depend from the method of claim 1 and the apparatus of claim 12, respectively. Claims 2 and 13 add the elements of first and second portions each comprising segments of the DRAM that are distinguishable. The Examiner asserted that the test cells of Burgan disclose these steps or elements.

Applicant responds that the test cells of Burgan identified by the Examiner in the remarks are not segments of a DRAM and are not distinguishable based on the segments. The Burgan test cells reside (in Figure 1 of Burgan) in the refresh control circuitry 20 and are not part of the memory array 12 addressed by the decoder 14, and are not distinguishable as claimed in Applicant's claims 2 or 13. Further and as an alternative basis for allowance, the claims depend from and incorporate the allowable elements of claims 1 and 12, and so are also allowable over the reference on that basis. In any event, Applicant concludes that the dependent claims are allowable over the reference. Reconsideration and allowance is therefore requested.

Claims 3 and 14 likewise depend from claims 1 and 12. These claims recite the first portion including subportions, the subportions being physically discontiguous. The Examiner asserts that the refresh control circuitry of Burgan as shown in Figure 3, discloses these elements.

Applicant replies that claim 3, for example, requires subportions of a portion of a DRAM, which includes a plurality of memory cells. Applicant believes that the test cells disclosed by Burgan are not subportions as recited in claim 3, as the test memory cells are allegedly the required portions, Applicant does not find disclosure in Burgan that the cells are then arranged as the required subportions of portions. Alternatively, as an additional basis for the allowance, claims 3 and 14 depend from and recite additional limitations on the allowable method steps or

limitations of claims 1 and 12, respectively. Applicant concludes that the dependent claims are allowable over the reference. Reconsideration and allowance is therefore requested.

Claims 4 and 15 were likewise rejected as anticipated by Burgan. Claim 4 recites in part:

> ...wherein said subportions are wordline spaces of said DRAM and said information allows said first portion and said second portion to be distinguished on the basis of said wordline spaces.

Applicant replies to Examiner's argument that the required element of the information allowing the first portion and second portion to be distinguished on the basis of said wordline spaces is not shown, taught or suggested by the Burgan reference. The information stored in the test cells, indicated in the Examiner's rejection of claims 1 and 12 as the "information" of Burgan that meets the claimed element of information, is not used to distinguish portions of a DRAM on the basis of wordline spaces. The wordlines of Figure 2 are merely single cell select lines from test controller circuitry. The information stored in the test cells is used only to monitor the leakage effects as it relates to the refresh rate of the test cells, not to distinguish any subportions based on wordline spaces. Accordingly, Applicant believes the dependent claims are allowable. Again, both claims 4 and 15 depend from and incorporate the allowable recitations of the parent claims 1 and 12. Both dependent claims are therefore also believed to be allowable on this basis as an alternative. Reconsideration and allowance are therefore requested.

Claims 6 and 17 depend from and recite the additional limitation that the information of claims 1 and 12 be stored in the DRAM. Without agreeing with the Examiner's apparent conclusion that by storing logic in test cells having a single capacitor as in Burgan, these elements are disclosed, Applicant submits that as these claims incorporate the allowable features of the parent claim, these dependent claims are also allowable. Reconsideration and allowance is

therefore requested.

Claim 8 was likewise rejected under § 102 over Burgan and the Examiner asserted the required storing of information on one or more fuses on an integrated circuit including said DRAM was met. The Examiner did not direct Applicant to any part of the reference specifically for the elements.

Anticipation under 35 U.S.C. § 102 requires that the reference disclose each element of the claim. Applicant replies that a simple word search of the Burgan reference reveals that the term "fuse" is not used anywhere. Accordingly, Applicant believes that the reference fails to show, teach or suggest the claimed method steps and that claim 8 is therefore allowable.

Alternatively, as argued above for the other rejected dependent claims, claim 8 also depends from and incorporates the method steps of claim 1 and is therefore also allowable over the rejection. Reconsideration and allowance are therefore requested.

Claims 9 and 20 were also rejected. Claim 9 adds a refresh of one to n portions at a first rate, a second rate and up to an nth rate. Claim 20 is analogous for the apparatus claims. The Examiner asserts Burgan discloses the claimed elements.

Applicant responds that Burgan discloses refreshing the DRAM array 12 at a single adaptable refresh rate based on monitoring the logic state of test cells located in the refresh circuitry. Applicant does not believe that the refreshing of the test cells of Burgan, each of which is described as having a single memory cell, which are located in a refresh controller, provides the required elements of claims 9 or 20. Applicant concludes these claims are allowable over the reference.

Claims 10 and 21 were also rejected over the Burgan reference. The Examiner asserts that the elements of "said information is stored in a space accessible through one or more lines of

said DRAM." The Examiner specifically recites Col. 4 at lines 39-48.

Applicant replies that the DRAM described by Burgan can indeed store information in the form of logical bits or data. Col. 4 lines 39-48 describe a conventional DRAM array. However, the claimed element of storing "said information" is not shown, taught or suggested by Burgan, which discloses refreshing a memory array at a single adjustable refresh rate. The information used to distinguish portions as recited in claims 1 and 12, which is now required in the recitations of dependent claims 10 and 21 to be stored in the DRAM, is not disclosed by Burgan.

Accordingly, Applicant believes that these claims are allowable over the rejection. Alternatively, and as submitted with respect to the other dependent claims, claims 10 and 21 depend from and incorporate the allowable elements of claims 1 and 12 as argued above and therefore these dependent claims are also believed to be allowable. Reconsideration and allowance are requested.

Claim 11 recites a post-fabrication stress test as a method step for determining the information recited. The Examiner asserts that a portion of the Burgan specification at Col. 4, lines 15-17, discloses the step.

Applicant responds that firstly, if Burgan discloses a "post-fabrication stress test," that answers the Examiner's question discussed above with respect to the § 112 rejection, as to whether the term is a term of art. It is. With respect to the Burgan reference and particularly with respect to the lines recited by the Examiner, Applicant finds no teaching of any stress test method or step at that location. Burgan does not disclose the method of claim 11 and therefore, Applicant believes that claim 11 is allowable over the reference. As an alternative reason for allowance, the claim depends from and incorporates the allowable method of claim 1, and is therefore also believed to be allowable. Reconsideration and allowance are requested.

Claims 5 and 16 were rejected under 35 U.S.C. § 103 as being unpatentable over Burgan in view of Klein. This rejection is hereby respectfully traversed.

The Examiner admits that the Burgan reference fails to teach the required active mode and sleep modes for the portions of the DRAM. Klein is added to provide the missing elements.

Applicant responds that as amended, claims 1 and 12, the parent claims are allowable over Burgan. Claims 5 and 16 depend from and incorporate the allowable elements of those claims and are therefore allowable over Burgan. The Klein reference does not cure the deficiencies of the Burgan reference and therefore these dependent claims are allowable over the relied upon combination as well. Reconsideration and allowance are therefore respectfully requested.

Claims 7 and 18-19 were likewise rejected under 35 U.S.C. §103 as being unpatentable over Burgan in view of Caulkins. This rejection is also hereby respectfully traversed.

With respect to claims 7 and 18, the Examiner remarks that Burgan fails to teach the required non-volatile memory for storage and accessing the non-volatile memory to store the "said information" in the DRAM. Caulkins is then combined to provide the missing non-volatile storage element.

Applicant responds that as amended, claims 1 and 12, the parent claims, are allowable over Burgan. Claims 7 and 18 depend from and incorporate the allowable elements of those claims and are therefore allowable over Burgan. The Caulkins reference does not cure the deficiencies of the Burgan reference and therefore these dependent claims are allowable over the relied upon combination as well. Reconsideration and allowance are therefore respectfully requested.

With respect to claim 19, the Examiner remarks that the Burgan reference discloses the

required fuses. This argument by the Examiner seems most closely related to the § 102 rejection of claim 8. As argued above, the Burgan reference does not use the term "fuse" and does not teach fuses as are known in the art anywhere. The Caulkins reference is not mentioned by the Examiner in the rejection. Applicant believes that claim 19 is allowable for the reasons given above with respect to claim 8. Further claim 19 is allowable for the alternative reason that it depends from and incorporates the apparatus elements of claim 12, which is allowable, and that the dependent claim is therefore also allowable over the rejection. Reconsideration and allowance are requested.

Applicant has made a diligent effort to place the claims in condition for allowance. However, should there remain unresolved issues that require adverse action, it is respectfully requested that the Examiner telephone Mark E. Courtney, Applicant's attorney, at 972-732-1001 so that such issues may be resolved as expeditiously as possible. No fee is believed due in connection with this filing. However, should one be deemed due, the Commissioner is hereby authorized to charge Deposit Account No. 50-1065.

Respectfully submitted,

11/18/05
Date

Mark E. Courtney
Attorney for Applicant
Reg. No. 36,491

Slater & Matsil, L.L.P.
17950 Preston Rd., Suite 1000
Dallas, Texas 75252-5793
Tel. 972-732-1001
Fax: 972-732-9218